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APPLICATION NOTE

Optical circulation loop measurement

ME7750A/ME7760A

43.5G bit/s BERT System

ANRITSU CORPORATION

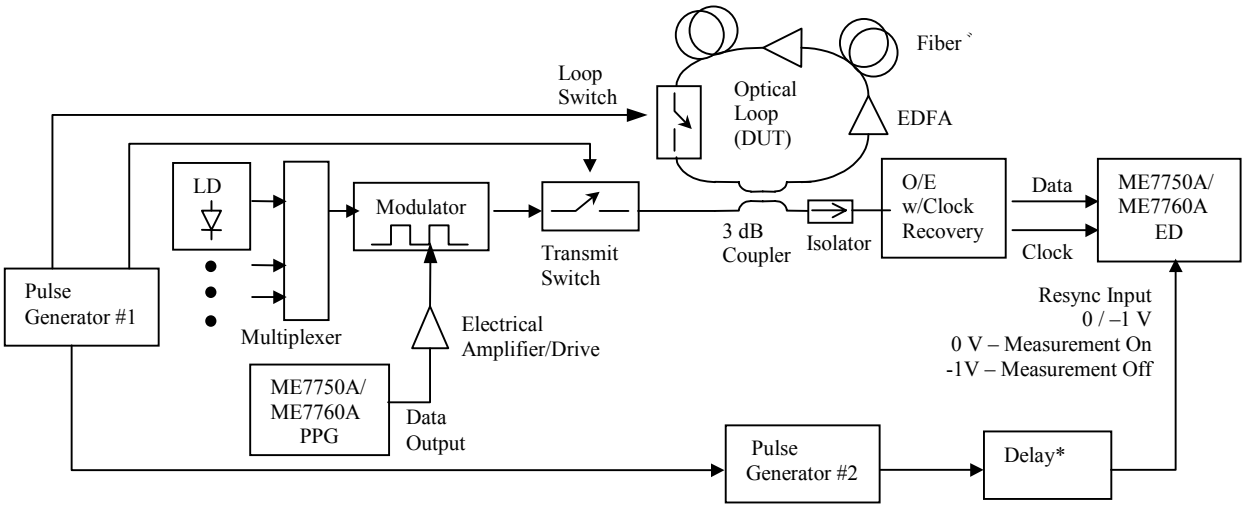
ME7750A/ME7760A for Circulating Loop Measurements

40G technologies are developed for MAN mainly, and also investigated for Long Haul networks.
Since there are some problems under Long Haul use, it is necessary to evaluate error ratio with using actual long optical network. Circulating Loop measurement is often used for such an evaluation of Long Haul, which emulates long optical line.

ME7750A/ME7760A 43.5Gigabit Error Detector (ED) should be the best solution for the demanding requirements of burst data measurements.
This note describes how ME7750A/ME7760A systems can be used in Circulating Loop experiments.

Circulating Loop Testing

Circulating Loop (also called "Optical Loop") testing has been performed since the late 1970's.
Initially the Optical Loop tests were used to characterize pulse propagation in early MM and SM fiber systems. A recent renewed interest in Circulating Loop testing has been fueled by R&D of OC-192/STM-64 rate (9,95328 Gb/s) transmission systems, dispersion compensating systems, Soliton transmission systems, EDFA based systems, and WDM systems. This technology is also used for 40G development. Optical Loop configurations allow designers to simulate long haul optical transmission system with just a fraction of the overall system hardware (fiber, optical amplifiers, filters, etc.). The designer benefits from reduced setup size, complexity, and cost. For example, an entire transpacific 10,000km system can be simulated in a lab using an Optical Loop setup consisting of only 400km of fiber and 8 optical amplifiers. By looping through the Optical Loop 25 times, the behavior of the full system can be evaluated. Circulating Loop experiments yield valuable information on the full system BER, eye diagram shape, dispersion, Signal-to-Noise ratio, and interchannel interaction of a WDM system. Figure 1 below shows a typical Circulating Loop test configuration.



*A separate Delay circuit is not required if Pulse Generator#2 has a "Trigger Delay" feature.

Figure 1: Circulating Loop Setup

Description of Circulating Loop Setup

A simplified description of the operation of a Circulating Loop setup is as follows.

The Pulse Pattern Generator (PPG)/modulator generates an optical gigabit data scream. Closing the Transmit Switch loads the data stream into the optical loop (via the 3 dB coupler). After the loop fills with data (the Loop Time), the Transmit Switch opens and the Loop Switch closes. The loaded bit stream then re-circulates around the loop. Each time around the loop the data passes through the coupler. The coupler directs a portion of the data to the O/E where the Error Detector (ED) monitors the BER of the bit stream. A delay circuit sets the distance range monitored by the ED. For clarification, a representative example is below.

A Circulating Loop is used to simulate an OC-192/STM-64 (9,95328 Gb/s) 10,000km system. The Loop consists of a DUT containing 8 EDFA's separated by 50km of fiber (total loop length=400km). The Loop Time, which is related to Loop Length by: Loop Time=Loop Length/Velocity of Light in Fiber, is 2ms (400km÷2E5km/s). The Loop Gain is adjusted to unity. The data must loop 25 times to simulate 10,000km. The total elapsed time for 25 loops is 50ms. The duty cycle of the data burst is 4% (2ms/50ms). Figure 2 shows the timing diagram for this example. To monitor the data quality at 6,000km the Delay circuit is set for 30ms (Loop 15).

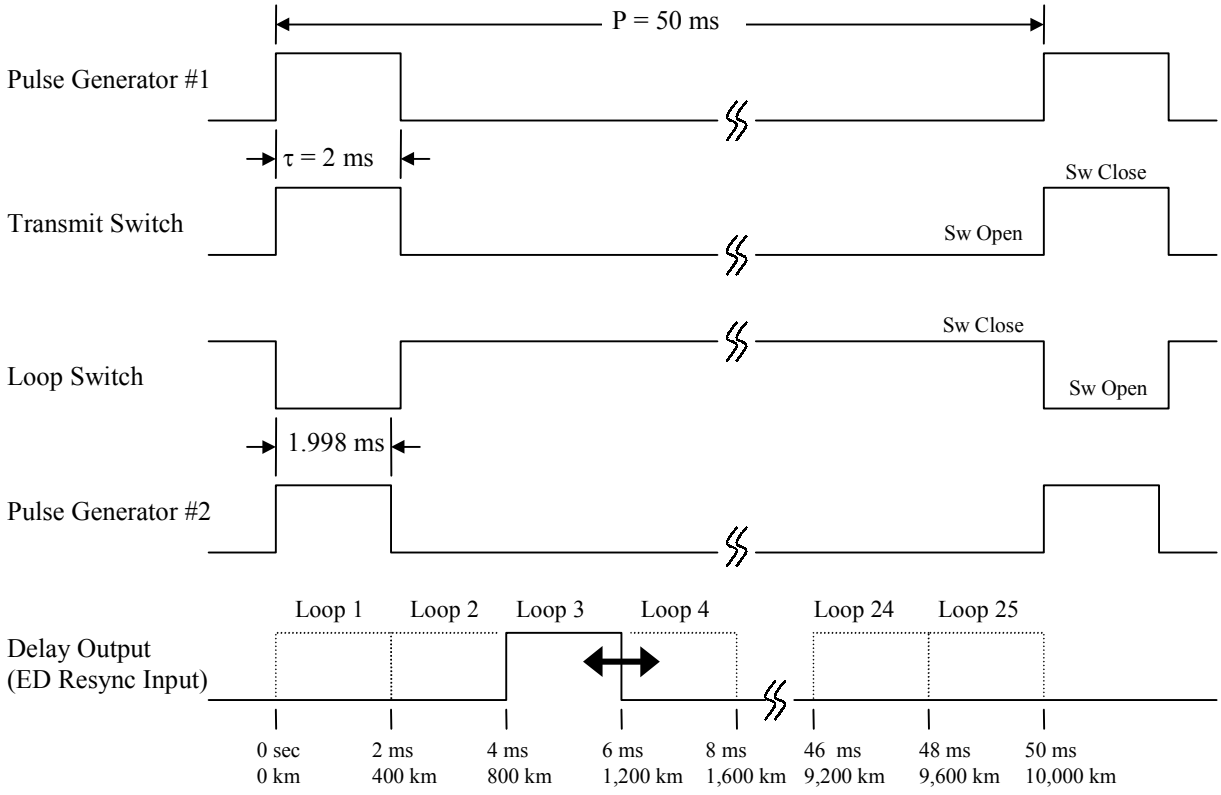


Figure 2: Example Circulating Loop Timing Diagram

Circulating Loop Components

Optical Loop: The Optical Loop consists of a representative portion of the overall transmission system. Typically, the DUT contains spans of fiber separated by optical amplifiers/isolators/filters. The minimum length of the loop (minimum loop time) is constrained by the sync time of the Error Detector. A sync time of approximately 1us is typical for a 10Gb/s rate. The maximum length of the loop is limited only by the user's resources. Generally, due to cost and part availability constraints, the user will opt for a loop setup which minimizes part count and fiber lengths while still representing of the overall transmission system.

The gain of the DUT loop is adjusted to equal 1. This allows the data to re-circulate without loss.

Pulse Generator #1: Provides synchronizing signals to the Loop Switch, Transmit Switch, PPG, and Pulse Generator #2. The Pulse width of PG#1, τ, is derived from the Loop Time. The period, P, is dependent on the maximum simulated distance.

Pulse Generator #2: This Pulse Generator is slaved to Pulse Generator #1. The pulse width setting of this unit is slightly less than τ to account for trailing edge switching transients. The trailing edge transient time is related to the fall time of the Transmit Switch. It is recommended that the PW of Pulse Generator #2 is 2us less than τ.

Pulse Generator #2 can act as a delay circuit if equipped with an "External Trigger Delay" feature. Adjust the Trigger Delay to monitor the appropriate Loop interval on the Error Detector.

Transmit Switch/Loop Switch: These switches must have low insertion loss, low polarization dependency, high extinction ratio, and small rise/fall times to minimize transients. The repetition rate of the switch is a function of the loop time. Typical repetition rates are in the kHz range.

O/E with Clock Recovery: This circuit converts the Optical Loop output signal to electrical DATA and CLOCK signals suitable for input into the Error Detector. The voltage levels into the Error Detector should be in the range 0.1 to 2.0 Vp-p (this is guaranteed input range; ED typically work properly for input levels around 70m Vp-p).

Pulse Pattern Generator side: The PPG provides the gigabit bit pattern that drives the optical modulator. The PPG data output must produce a high quality eye diagram, i.e. fast rise/fall times, low distortion, low jitter, and high Q factor[2] (minimal noise on the eye "rails").

Error Detector side: The ED must be able to synchronize quickly on incoming burst data. An Error Detector cannot make valid error measurements until synchronization is achieved. Circulating Loop tests are not possible if the sync time approaches or exceed the duration of the burst data. Both ME7750A and ME7760A can synchronize to input pattern quickly, which is standard PRBS and PRGM.

Typical values for synchronization times are given in Table 1.

Independent mode

Bit Rate	PRBS Sync Time	PRGM Sync Time (Zero-sub pattern)
8G - 32Gbit/s	< 5.0 us	Not specified
32G – 43.5Gbit/s	< 2.0 us	< 100 us

*Threshold error ratio of synchronization is less than 1E-2

Table1: Synchronization Times for ME7750A/ME7760A

4ch Combined mode

Bit Rate	PRBS Sync Time	PRGM Sync Time (Zero-sub pattern)
8G - 32Gbit/s	< 5.0 ms	Not specified
32G – 43.5Gbit/s	< 2.0 ms	< 10 ms

* Threshold error ratio of synchronization is less than 1E-2

Table 1-2: Synchronization Times for ME7750A/ME7760A

ME7750A/ME7760A does not require a continuous "local" clock signal during burst measurements. Only the burst clock recovered by the O/E is necessary.

LD, Multiplexer, Modulator, and Electrical Amplifier: The LD is typically a DFB operating in the 1310nm or 1550nm window. Multiple 1550nm band DFB sources can be used in conjunction with a multiplexer to simulate WDM channels. Each DFB is modulated either directly or externally with a Lithium Niobate or EO modulator. An external electrical amplifier/driver is then required when the maximum PPG output of 2Vp-p is not sufficient to drive the modulator. Anritsu offers complete line of Wideband Amplifiers and High Speed Drivers that boost the PPG output with minimal distortion (see the Anritsu High Speed Devices Catalog).

ME7750A/ME7760A Setup for Circulating Loop Measurements

Following are setting condition of PPG.

- The desired bit rate is set by adjusting the clock rate of the external synthesizer.
- The test Pattern is set to PRBS or DATA (a user defined pattern). If DATA is selected, input the user pattern via front panel manual input, GPIB interface, or floppy disk. It is useful for setting PRGM pattern to use MX177601A SDH/SONET pattern editor, which can edit SDH/SONET pattern and user defined pattern. The pattern is sent from PC to the ME7750A/ME7760A by GPIB or FD.
- The amplitude of the data output is 2.0 Vp-p fixed. A DC offset is also selectable to use external bias network, because output circuit is AC coupling.

Following are setting condition of ED.

- Burst measurement requires gating signal which shows enable time for measurement. This signal should connect to the MP1776A (ED).
- Set the test pattern to PRBS or Data. For PPG patterns, select the same pattern that is chosen on the PPG, i.e.2^{15} -1, 2^{23} -1 etc. When it is necessary to use PRGM pattern, we recommend to use the ME7760A. Because the ME7760A can set longer pattern than ME7750A.
- Adjust the Threshold and Delay Time values manually to locate the "center of the eye". Note: the AUTO SEARCH function does not work properly with burst data.
- Verify that the input data into the MP1802A is greater than 100mV p-p (minimum sensitivity)

*1 For an additional information on Circulating Loop Experiments refer to:
Bergano, N. S, C. R. Davidson, Circulating Loop Experiments for the Study of Long-Haul Transmission Systems Using Erbium-Doped Fiber Amplifiers, Journal of Lightwave Technology, Vol. 13, No. 5, May 1995

*2 For an additional information on Q factor (Quality factor) refer to:
Bergano, N. S., F. W. Kerfoot, and C. R. Davidson, Margin Measurements in Optical Amplifier Systems, IEEE Photonics Technology Letters, Vol. 5, No 3, March 1993.

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Specifications are subject to change without notice.

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